

WHAT IS CLAIMED IS:

1. For use in a processor having separate instruction and
2 data buses, separate instruction and data memories and separate
3 instruction and data units, a mechanism for supporting self-
4 modifying code, comprising:

5 a crosstie bus coupling said instruction bus and said data
6 unit; and

7 a request arbiter, coupled between said instruction and data
8 units, that arbitrates requests therefrom for access to said
9 instruction memory.

2. The mechanism as recited in Claim 1 wherein said data
unit can employ said instruction memory to contain data.

2. The mechanism as recited in Claim 1 wherein said request
arbiter gives a higher priority to requests from said data unit.

4. The mechanism as recited in Claim 1 further comprising an
2 instruction prefetch mechanism that prefetches instructions from a
3 said instruction memory into an instruction cache, said request
4 arbiter stalling said prefetch mechanism when said request arbiter
5 grants a request from said data unit for said access to said
6 instruction memory.

5. The mechanism as recited in Claim 3 wherein at least some
2 instructions prefetched into said instruction cache are invalidated
3 when said request arbiter grants said request.

6. The mechanism as recited in Claim 4 wherein a
2 programmable control register is employed to invalidate said at
3 least some instructions.

7. The mechanism as recited in Claim 1 wherein said
2 instruction memory is a local instruction memory and said processor
3 further comprises an external memory interface.

8. The mechanism as recited in Claim 1 wherein said
2 processor is a digital signal processor.

9. A method of supporting self-modifying code in a processor

2 having separate instruction and data buses, separate instruction
3 and data memories and separate instruction and data units,
4 comprising:

5 arbitrating requests from said instruction and data units for
6 access to said instruction memory; and

7 communicating instructions between said instruction bus and
8 said data unit via a crosstie bus extending therebetween.

10. The method as recited in Claim 9 wherein said data unit

2 can employ said instruction memory to contain data.

11. The method as recited in Claim 9 wherein said arbitrating

2 comprises giving a higher priority to requests from said data unit.

12. The method as recited in Claim 9 further comprising:

2 prefetching instructions from a said instruction memory into
3 an instruction cache; and

4 stalling said prefetch mechanism when a request from said data
5 unit for said access to said instruction memory is granted.

13. The method as recited in Claim 12 further comprising

2 invalidating at least some instructions prefetched into said
3 instruction cache when said request is granted.

14. The method as recited in Claim 13 wherein a programmable
2 control register is employed to invalidate said at least some
3 instructions.

15. The method as recited in Claim 9 wherein said instruction
2 memory is a local instruction memory and said processor further
3 comprises an external memory interface.

16. The method as recited in Claim 9 wherein said processor
2 is a digital signal processor.

17. A digital signal processor, comprising:

2 an execution core having an instruction cache;

3 a memory unit coupled to said execution core and having

4 separate instruction and data buses, separate instruction and data

5 memories and separate instruction and data units;

6 a crosstie bus coupling said instruction bus and said data

7 unit; and

8 a request arbiter, coupled between said instruction and data

9 units, that arbitrates requests therefrom for access to said

10 instruction memory.

18. The digital signal processor as recited in Claim 17

2 wherein said data unit can employ said instruction memory to

3 contain data.

19. The digital signal processor as recited in Claim 17

2 wherein said request arbiter gives a higher priority to requests

3 from said data unit.

20. The digital signal processor as recited in Claim 17

2 further comprising an instruction prefetch mechanism that

3 prefetches instructions from a said instruction memory into said

4 instruction cache, said request arbiter stalling said prefetch

5 mechanism when said request arbiter grants a request from said data

6 unit for said access to said instruction memory.

21. The digital signal processor as recited in Claim 20
2 wherein at least some instructions prefetched into said instruction
3 cache are invalidated when said request arbiter grants said
4 request.

22. The digital signal processor as recited in Claim 21
2 wherein a programmable control register is employed to invalidate
3 said at least some instructions.

23. The digital signal processor as recited in Claim 17
2 wherein said instruction memory is a local instruction memory, said
3 data memory is a local data memory and said memory unit further has
4 an external memory interface.